INTL9546 Product Brief

1. Description

The INTL9546 is a quad bidirectional translating switch controlled via the I2C-bus. The SCL/SDA upstream pair fans out to four downstream pairs, or channels. Any individual SCx/SDx channel or combination of channels can be selected, determined by the contents of the programmable control register.

An active LOW reset input allows the INTL9546 to recover from a situation where one of the downstream I2C-buses is stuck in a LOW state. Pulling the $\overline{\text{}}$("RESET") pin LOW resets the I2C-bus state machine and causes all the channels to be deselected as does the internal Power-On Reset (POR) function.

The pass gates of the switches are constructed such that the VDD pin can be used to limit the maximum high voltage which is passed by the INTL9546. This allows the use of different bus voltages on each pair, so that 1.8 V or 2.5 V or 3.3 V parts can communicate with 5 V parts without any additional protection. External pull-up resistors pull the bus up to the desired voltage level for each channel. All I/O pins are 5 V tolerant.

2. Applications

- Servers
- Routers (Telecom Switching Equipment)
- Factory Automation
- Products with I2C Slave Address Conflicts

3. Key Features

- of-4 bidirectional translating switches
- I2C-bus interface logic; compatible with SMBus standards
- Active LOW reset input
- 3 address pins allowing up to 8 devices on the I2C-bus
- Channel selection via I2C-bus, in any combination
- Power-up with all switch channels deselected
- Low Ron switches
- Allows voltage level translation between 1.8 V, 2.5 V, 3.3 V and 5 V buses
- No glitch on power-up
- Supports hot insertion
- Low standby current
- Operating power supply voltage range of 1.65 V to 5.5 V
- 5 V tolerant Inputs
- 0 Hz to 400 kHz clock frequency
- ESD protection exceeds 4000 V HBM per JESD22-A114 and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JEDEC Standard JESD78 which exceeds 150 mA

4. Functional Diagram

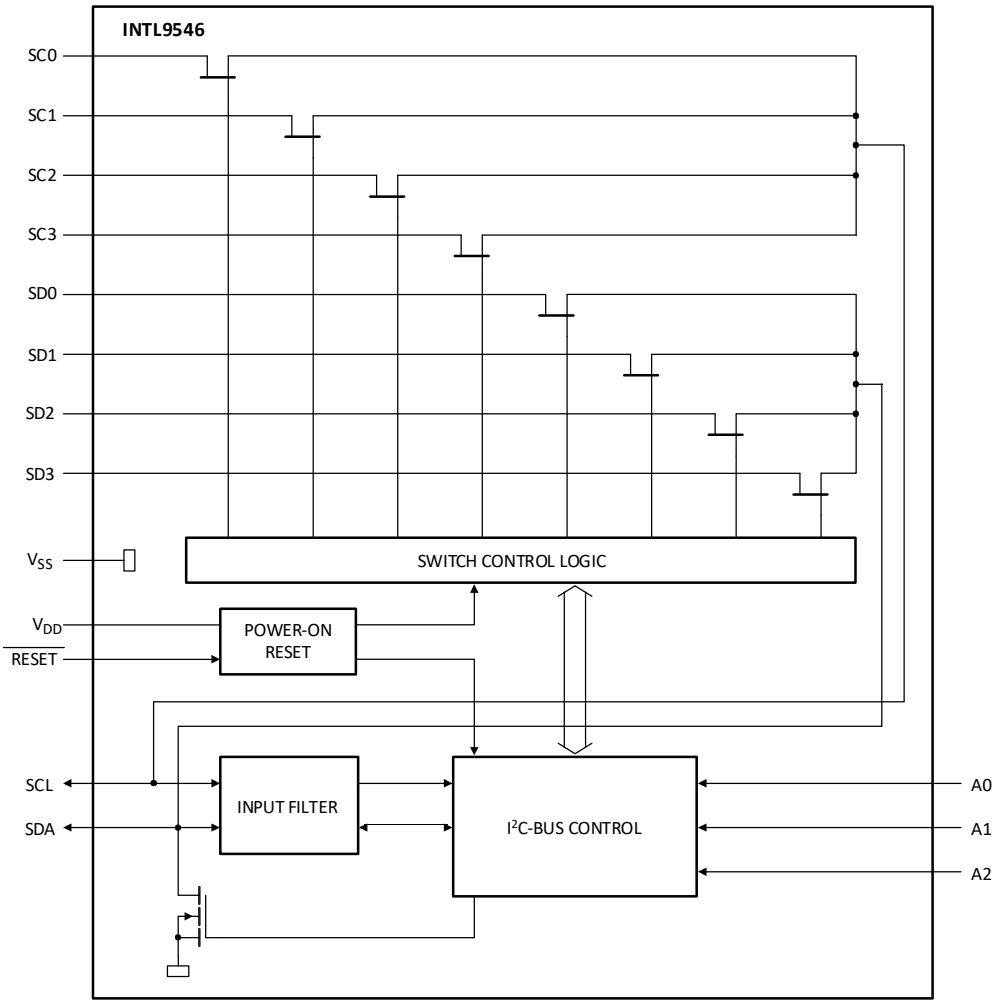

Figure 1 Functional Diagram

5. Pin Maps

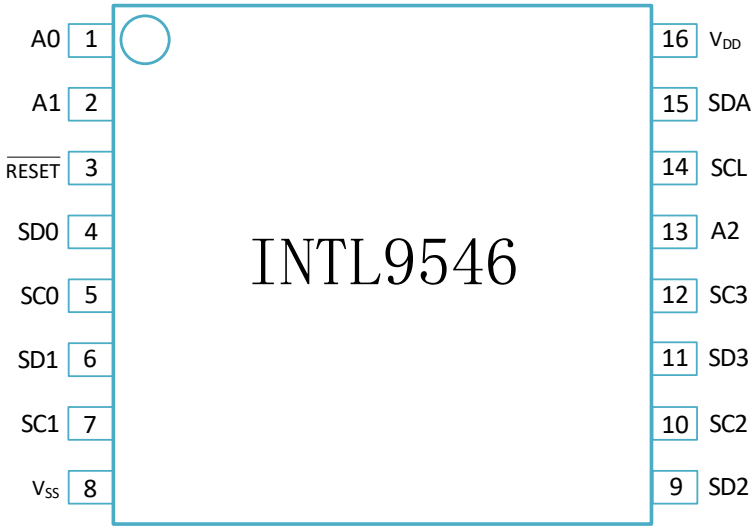

Figure 2 Pin Assignment Diagram

6. Pin Descriptions

Table 1 Pin Descriptions

Symbol	Pin	Description
A0	1	address input 0
A1	2	address input 1
$\overline{RESET}$	3	active LOW reset input
SD0	4	serial data 0
SC0	5	serial clock 0
SD1	6	serial data 1
SC1	7	serial clock 1
V_{SS}	8	supply ground
SD2	9	serial data 2
SC2	10	serial clock 2
SD3	11	serial data 3
SC3	12	serial clock 3
A2	13	address input 2
SCL	14	serial clock line
SDA	15	serial data line
V_{DD}	16	supply voltage